PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 5 : G06F 13/40 | A1

(11) International Publication Number: WO 94/19749

(43) International Publication Date: 1 September 1994 (01.09.94)

(21) International Application Number: PCT/US93/10351

(22) International Filing Date: 27 October 1993 (27.10.93)

(30) Priority Data:
08/023,577 26 February 1993 (26.02.93) US

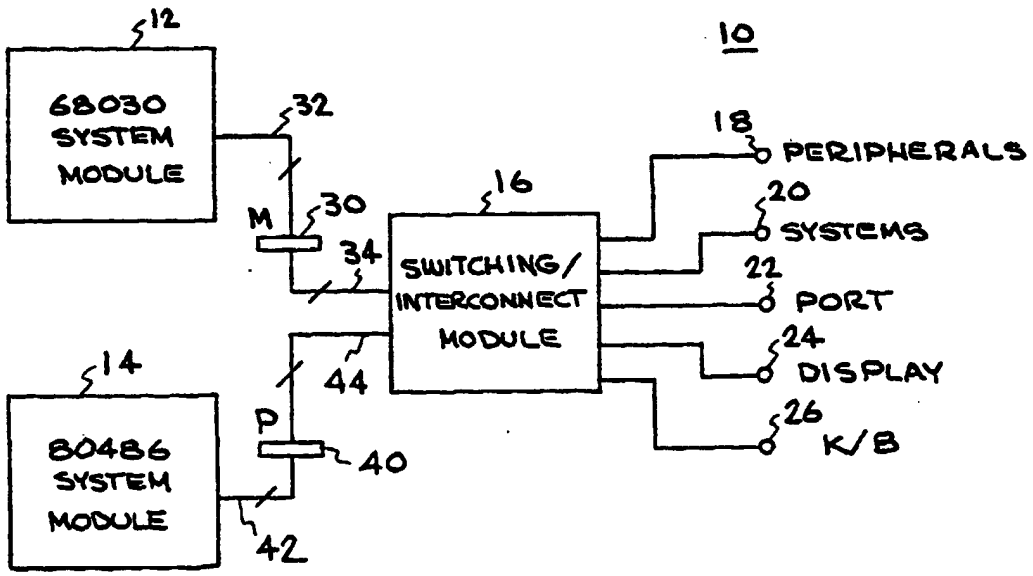
(71)(72) Applicant and Inventor: CHOU, Benjamin, E. [US/US]; 20323 Glen Brae Drive, Saratoga, CA 95070 (US).

(74) Agent: KING, Patrick, T.; Law Offices of Patrick T. King, 32 Seascape Village, Aptos, CA 95003 (US).

(81) Designated States: AU, BR, CA, FI, JP, KR, NO, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE).

Published
With international search report.

(54) Title: COMPUTER SYSTEM FOR SHARING COMMON SYSTEM RESOURCES WITH TWO OR MORE INDEPENDENTLY OPERATING MICROCOMPUTERS



(57) Abstract

A microcomputer system (10) switchably connects two or more different, fully functional CPU-based microprocessor systems designs, such as MacIntosh™-compatible (12) and PC-compatible (14) systems, to alternatively shared common system resources. These shared common system resources include, for example, a video display, user input means such as a keyboard or a mouse, a sound port, main memory, and input/output (I/O) means such as a modem or printer. The system according to the invention also provides for a second set of dedicated system resources to the microcomputer system. In a MAC-compatible/PC-compatible scheme, the second set of dedicated system resources includes, for example, a floppy disk drive (134) compatible with either system as well as NUBUS slots (50) and ISA slots (94).

A0

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AT	Austria	**GB**	United Kingdom	**MR**	Mauritania
AU	Australia	**GE**	Georgia	**MW**	Malawi
BB	Barbados	**GN**	Guinea	**NE**	Niger
BE	Belgium	**GR**	Greece	**NL**	Netherlands
BF	Burkina Faso	**HU**	Hungary	**NO**	Norway
BG	Bulgaria	**IE**	Ireland	**NZ**	New Zealand
BJ	Benin	**IT**	Italy	**PL**	Poland
BR	Brazil	**JP**	Japan	**PT**	Portugal
BY	Belarus	**KE**	Kenya	**RO**	Romania
CA	Canada	**KG**	Kyrgystan	**RU**	Russian Federation
CF	Central African Republic	**KP**	Democratic People's Republic of Korea	**SD**	Sudan
CG	Congo			**SE**	Sweden
CH	Switzerland	**KR**	Republic of Korea	**SI**	Slovenia
CI	Côte d'Ivoire	**KZ**	Kazakhstan	**SK**	Slovakia
CM	Cameroon	**LI**	Liechtenstein	**SN**	Senegal
CN	China	**LK**	Sri Lanka	**TD**	Chad
CS	Czechoslovakia	**LU**	Luxembourg	**TG**	Togo
CZ	Czech Republic	**LV**	Latvia	**TJ**	Tajikistan
DE	Germany	**MC**	Monaco	**TT**	Trinidad and Tobago
DK	Denmark	**MD**	Republic of Moldova	**UA**	Ukraine
ES	Spain	**MG**	Madagascar	**US**	United States of America
FI	Finland	**ML**	Mali	**UZ**	Uzbekistan
FR	France	**MN**	Mongolia	**VN**	Viet Nam
GA	Gabon				

COMPUTER SYSTEM FOR SHARING COMMON SYSTEM RESOURCES WITH TWO OR MORE INDEPENDENTLY OPERATING MICROCOMPUTERS

BACKGROUND OF THE INVENTION

1. Technical Field. This invention relates to microcomputer systems and, more particularly, to microcomputer systems which include two or more independent microcomputers of different types, each operating with its own software and switchably sharing common system resources.

2. Background Art. Currently existing microcomputers attempt to provide for flexibility of use using techniques such as software emulation or hardware add-on adapter cards. In software emulation a computer system of one type has software for emulating the operation of a second type of system. Emulators provide programming techniques and/or special machine features which permit a given computer system to execute programs written for another system. These emulation systems

are often slow in operation. Add-on adapter cards are circuit cards which plug into a host system computer system and permit the host computer system to provide some of the functions of another computer system. These ad-hoc techniques have disadvantages such as performance degradation and restricted software compatibility.

The need has arisen for a microcomputer system which economically combines two or more different CPU-based independent operating systems, such as MacIntosh-compatible and PC-compatible operating systems, in a cost-effective and space-effective manner.

DISCLOSURE OF THE INVENTION

It is therefore an object of the invention to provide a microcomputer system which links two or more different, fully functional CPU-based microprocessor systems designs, such as MacIntosh-compatible and PC-compatible systems, to common system resources. These common system resources include, for example, a video display, user input means such as a keyboard or a mouse, a sound port, main memory, and input/ output (I/O) means such as a modem or printer. The system according to the invention also provides for a second set of dedicated system resources to the microcomputer system. In a MAC-compatible/PC-compatible scheme, the second set of dedicated

system resources includes, for example, a floppy disk drive compatible with either system as well as NUBUS slots and ISA slots.

This system provides a user with maximum convenience and flexibility. A user can switch the common system resources to either system at will. The software and hardware features of either microcomputer system are readily activated with a hardware or software switch. This system minimizes cost by sharing in common as many peripheral devices as possible between the two or more different CPU-based microprocessor systems.

In accordance with this and other objects of the invention, a microcomputer system is provide according to the invention for alternatively sharing common system resources between two independent microcomputer systems. A first independent microcomputer system is provided which runs software of a first type, for example, MacIntosh software. A second independent microcomputer system is provided which runs software of a second type, for example, IBM PC software. The first independent microcomputer system can be a MacIntosh-compatible microcomputer system operating with MacIntosh-compatible software with a MacIntosh-compatible boot read-only-memory ROM. The second independent microcomputer system includes a PC-compatible microcomputer system operating with PC-compatible software.

Switchable means are provide for sharing a first set of common system resources with the two independent microcomputer systems. A second set of system resources is connected to the first and the second independent microcomputer system. The switchable means includes either hardware switch means or software switch means.

The system includes means for connecting the first independent microcomputer system to the first set of common system resources and for booting up the first independent microcomputer system with the first set of common system resources connected thereto. The system also includes means for connecting the second independent microcomputer system to the first set of common system resources and for booting up the second independent microcomputer system with the second set of common system resources connected thereto. To keep each system running when the common system resources are not available the system includes means for maintaining operation of the first and the second independent microcomputer systems when the common system resources are not connected respectively thereto.

The switchable means includes a number of ports and related circuitry for sharing a first set of common system resources. The switchable means includes a video port for connection to a video display and switch means for selectably

connecting a respective video signal either from the first independent microcomputer system or from the second independent microcomputer system to the video port. The switchable means includes: an audio port and switch means for selectably connecting a respective audio signal from the first independent microcomputer system or from the second independent microcomputer system to the audio port. One or more user input ports are provided with switch means for selectably connecting a respective user input signal from the user input port to either the first independent microcomputer system or to the second independent microcomputer system. One of the user input port s can include a keyboard port or a mouse port. The switchable means includes one or more serial communication ports. and a transceiver for receiving serial communication signals from either the first independent microcomputer system or from the second independent microcomputer system. The serial communication ports includes a modem port or a printer port. The switchable means can also include a main memory port.

The means for connecting a second set of system resources to the first and the second independent microcomputer system includes one or more connector slots for connecting respective plug-in cards for the first and the second independent microcomputer systems, including connector slots for a NUBUS bus system or for an ISA bus system. The means for connecting a second set of system resources to the first and the second

independent microcomputer system includes terminals for one or more floppy disk drives compatible with the first and the second independent microcomputer systems.

A method is provided according to the invention for alternatively sharing common system resources with two independent microcomputer systems. The method includes the steps of: connecting a first microcomputer system to the common system resources using switchable connection means; booting up the first microcomputer system with the common system resources being connected thereto; removing the common system resources from the first microcomputer system; maintaining the first microcomputer system operational with the common system resources being removed therefrom; connecting a second microcomputer system to the common system resources using switchable connection means; booting up the second microcomputer system with the common system resources being connected thereto; maintaining the second microcomputer system operational with the common system resources being removed therefrom; and activating the switchable connection means to selectably connect the common system resources to either the first microcomputer system or to the second microcomputer system.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and form a part of this specification, illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention:

FIGURE 1 is an overall system block diagram showing two independent microcomputer systems and a switching module for switchably sharing common system resources and for connecting dedicated resources to a particular microcomputer.

FIGURE 2 shows a more detailed block diagram of a switching module.

FIGURE 3 shows a block diagram of an exemplary first independent microcomputer system, such as a MacIntosh-compatible system.

FIGURE 4 shows a block diagram of an exemplary second independent microcomputer system, such as a PC-compatible system.

FIGURE 5 shows a simplified flow chart for booting one of the independent microcomputer systems.

FIGURE 6 shows a simplified flow chart for handling system operation such as switch interrupts and peripheral requests.

BEST MODE FOR INDUSTRIAL APPLICATION

Reference will now be made in detail to the preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. While the invention will be described in conjunction with the preferred embodiments, it will be understood that they are not intended to limit the invention to these embodiments. On the contrary, the invention is intended to cover alternatives, modifications and equivalents, which may be included within the spirit and scope of the invention as defined by the appended claims.

One implementation example is shown herein below as a particular exemplary design which is described herein below. This particular exemplary design integrates two popular microcomputers, the Intel 80X86 CPU based PC design and a Motorola 680X0 CPU based design into a single microcomputer system. This dual-microcomputer design uses common peripheral devices and support elements to minimize the cost of hardware and to provide for maximum usage of the hardware/software applications from each family of microcomputer designs. This specific example illustrates a new and original type of microcomputer system, previously unknown, which has the advantages of each microcomputer while providing for switched sharing of certain commonly used system resources.

FIGURE 1 shows a microcomputer system 10 according to the invention for alternatively sharing common system resources between two or more independently operating microcomputer systems. For illustration purposes two particular microcomputer systems are shown. A first independent microcomputer system 12, such a system based on a Motorola 68030 microprocessor system and a second independent microcomputer system 14, such as a system based on an Intel 80486 microprocessor is also shown. A switching/interconnection module 16 functions as an interface circuit between the two independent microcomputer systems and a number of I/O ports 18, 20, 22, 24, 26. Port 18 is connected to external peripheral devices, such as, for example, a printer or a modem. Port 20 is connected to external system components, such as, for example, a main memory. Port 22 provides an external port, such as for a NUBUS or ISA bus. Port 24 is connected to an external display devices, such as, for example, a display screen. Port 26 is connected to external user input device, such as, for example, a keyboard and/or a mouse.

A bridge connector M 30 provides an interface between an interconnection bus 32 for the 68030-based system 12 and an interconnection bus 34 connected to the switching/interconnection module 16. A bridge connector P 40 provides an interface between an interconnection bus 42 for the 80486-based system 14 and an interconnection bus 44 for the switching/interconnection module 16.

FIGURE 2 shows a more detailed block diagram of the switching/interconnection module 16. A number of MAC-compatible busses run from the bridge connector M to various elements of the bridge connector M. The bridge connector M provides a direct connection to NUBUS slots 50 for a MAC-compatible system. A serial communication controller bus A 52 is connected to a port of a transceiver circuit 54. A serial communication controller bus B 56 is switchably connected through a two-input multiplexer 58 to another port of the transceiver circuit 54. The other input port of the two-input multiplexer 58 is connected to a SERIAL COM2 bus 60 which runs to the bridge connector P for the 80486-based system 14.

A control terminal 62 for the two-input multiplexer 58 is operated with a manually-operated mechanical switch located, for example on the outside of the enclosure for the system 10, where the enclosure is, for example, a conventional PC mini-tower. The two-input multiplexer 58 can also be operated with an electro-mechanical or a software switch, as desired. In a similar manner, the other multiplexers which operate as selection switches and the analog switches, as described herein below, are operated, either manually, electromechanically, or under software control.

The transceiver circuit 54 has output signal lines connected, for example, to a modem port 64 or a printer port 66, as illustrated.

A low impedance analog switch 70 with a control terminal 72 is connected to a Mac keyboard/ mouse bus 74 connected to the bridge connector M and a PC keyboard/mouse bus 76 connected to the bridge connector P. The low impedance analog switch 70 has output buses connected respectively to a mouse port 78 and a keyboard port 80.

A digital-to-analog (D/A) converter and amplifier unit 82 has a sound port 84 at its output terminal. Its input terminal is connected to the output terminal of a two-input multiplexer 86 which has a control terminal 88. The input terminals of the two-input multiplexer 86 are connected to a Mac sound bus 90 and a PC sound bus 92.

ISA BUS slots 94 are connected through an ISA bus 94 to the bridge connector P for the 80486-based system 14.

A low impedance analog switch 100 with a control terminal 102 has its output terminal connected to a video port 104. The input terminals of the switch 100 are connected to a Mac video bus 106 and a PC video bus 108. The PC video bus 108 connects to the output terminals of a PC RAMDAC 110. PC video information is sent from the PC system on the ISA bus 94 to a video controller 112. The video controller 112 is connected through a VGA_RAM control bus 114 and a data/address bus 116 to a video RAM 118 for the PC system. The video controller 112 is connected through a

VGA_RAMDAC control bus 120 and a VGA pixel bus 122 to the RAMDAC 110.

A floppy disk drive A terminal 130 and a floppy disk drive B terminal 132 are connected through a floppy disk bus 134 to the bridge connector P, as illustrated.

FIGURE 3 shows a block diagram of the illustrative MAC-compatible 68030-based microcomputer system 12. The system includes as a CPU 150 a Motorola 68030; 32-bit internal architecture running at a 33 MHz clock speed with data, address, and control buses as illustrated in the Figure. An optional floating-point co-processor 152 includes Motorola 68882 numeric coprocessor operating at 33 MHz. Main memory for this MacIntosh-compatible processor includes a DRAM 154, which is expandable from 2 MBytes to 128 MBytes using industry standard 30-pin SIMM modules running at 70 nS speed or better and supporting 256KB, 1MB, 4MB, and 16 MBytes. 2M Bits of ROM are supplied.

For video memory, a 1 MByte DRAM video memory 156 is supplied with Fast Page capability.

Internal storage which is shared by both microcomputer systems 12, 14 included a system included in the I/O controller unit 158 for running a 3 1/2" FlexDisk drive, which can run

standard Apple 800K or 1.4M disks or PC 720K or 1.44M floppy disks.

For the MacIntosh-compatible processor, a SCSI/SCC controller unit 160 provides a 50-pin header SCSI external SCSI connector and an internal SCSI bus 162. One floppy disk drive is connected through a bus 162.

As shown in Figure 2, external connections shared by both processors include an IBM Ps/2 compatible keyboard connector at port 80 and an IBM Ps/2 compatible mouse connector at port 78. Video port 104 includes a D-type 15-pin video connector for PC VGA which can connect to a MacIntosh-compatible monitor with an adapter cable.

For the MacIntosh-compatible processor a DB-25, Apple MacIntosh compatible pinout SCSI connector, a modem port, and an RS422 serial port are provided.

Other system 12 units include a boot ROM 164, a bus controller 166, a memory controllers A & B, 168, 170, the I/O controller 158, a CRT controller 172, a RAMDAC 174, a keyboard/mouse controller 176, the SCSI controller 160, and a real time clock unit 178.

FIGURE 4 shows a block diagram of the 80486-based microcomputer system 14. Main memory 182 includes a DRAM,

expandable from 1 MBytes to 32 MBytes with Fast Page capability and page mode interleave.. A cache memory is provided with write back or write through architecture.. Video memory includes 1 MBytes DRAM video memory with Fast Page. Shared by both processors are the 3 1/2" FlexDisk drive which can run standard Apple 800K or 1.4M or PC 720K or 1.44M floppy disks. For the PC processor and IDE connector and one 5 1/4" or 3 1/2" disk drive car available.

With reference to Figure 2, external connectors shared by both processors 12, 14 includes the IBM Ps/2 compatible keyboard connector at port 80, the IBM Ps/2 compatible mouse connector at port 78, and the D-type 15-pin video connector for PC VGA at port 104. A 9-pin serial port is provided on COM 2 and a 25-pin parallel port LPT 1 is provided. Two 16-bit ISA slots 94 are provided.

Other system units include a CPU/CACHE/DRAM/AT BUS controller 184, an instruction processor controller IPC unit 186, an IDE/floppy disk controller and serial/parallel converter 188, a keyboard/mouse controller 190, an EPROM BIOS unit 192 and the ISA bus 194.

FIGURE 5 shows a simplified flow chart 200 for checking the availability of common peripheral devices or functions, such as SCSI, for one of the independent microcomputer systems at initial boot time. Block 202 indicates that the boot routine has been

called for. Decision block 202 determines whether the required common peripheral devices or function is available. If not, the system will loop through path 206 until availability is obtained. If availability is obtained, the system will follow path 208 to the block 210 which indicates that booting will continue. The software for each system is modified to enable the systems, once booted, to continue to operate, even when certain system resources, such as a screen or keyboard are not connected.

FIGURE 6 shows a simplified flow chart 220 for handling system operations such as switch interrupts and peripheral requests. Entry point 220 in entered when a hardware (or software) switch is activated. Block 222 causes the commonly shared peripherals, main memory, or SCSI operations to be handled properly to complete operations for one microcomputer system and to start operations for the other system. After the peripherals are handled for the one system, block 224 indicates that the system moves to handle the other microcomputer system requirements.

Figure 6 also shows a simplified flow chart for handling peripheral requests, which are indicated by the entry point 226. The availability of the peripheral is monitored by the decision block. If the common peripheral device is not available, path 232 indicates that the system will loop until the common peripheral device is available. Path 232 indicates that when the common

peripheral device is available, the system will continue as indicated by block 234.

The foregoing descriptions of specific embodiments of the present invention have been presented for purposes of illustration and description. They are not intended to be exhaustive or to limit the invention to the precise forms disclosed, and obviously many modifications and variations are possible in light of the above teaching. The embodiments were chosen and described in order to best explain the principles of the invention and its practical application, to thereby enable others skilled in the art to best utilize the invention and various embodiments with various modifications as are suited to the particular use contemplated. It is intended that the scope of the invention be defined by the Claims appended hereto and their equivalents.

IN THE CLAIMS:

1. A microcomputer system for alternatively sharing common system resources between two independent microcomputer systems, comprising:

a first independent microcomputer system, which has I/O terminals and which runs software of a first type;

a second independent microcomputer system, which has I/O terminals and which runs software of a second type;

switchable means, having a first set of terminals connected to the I/O terminals of the first independent microcomputer system and having a second set of terminals connected to the I/O terminals of the second independent microcomputer, for sharing a first set of common system resources.

2. The system of Claim 1 including means for connecting a second set of system resources to the first and the second independent microcomputer system.

3. The system of Claim 1 wherein the switchable means for sharing a first set of common system resources includes hardware switch means.

4. The system of Claim 1 wherein the switchable means for sharing a first set of common system resources includes software switch means.

5. The system of Claim 1 including:

means for connecting the first independent microcomputer system to the first set of common system resources and for booting up the first independent microcomputer system with the first set of common system resources connected thereto;

means for connecting the second independent microcomputer system to the first set of common system resources and for booting up the second independent microcomputer system with the second set of common system resources connected thereto.

6. The system of Claim 6 including means for maintaining operation of the first and the second independent microcomputer systems when the common system resources are not connected respectively thereto.

7. The system of Claim 1 wherein the first independent microcomputer system includes a MacIntosh-compatible microcomputer system operating with MacIntosh-compatible software.

8. The system of Claim 7 wherein the MacIntosh-compatible microcomputer system operating with MacIntosh-compatible software includes a MacIntosh-compatible boot read-only-memory ROM.

9. The system of Claim 1 wherein the second independent microcomputer system includes a PC-compatible microcomputer system operating with PC-compatible software.

10. The system of Claim 1 wherein the switchable means for sharing a first set of common system resources includes:

a video port for connection to a video display;

switch means for selectably connecting a respective video signal either from the first independent microcomputer system or from the second independent microcomputer system to the video port.

11. The system of Claim 1 wherein the switchable means for sharing a first set of common system resources includes:

an audio port;

switch means for selectably connecting a respective audio signal from the first independent microcomputer system or from the second independent microcomputer system to the audio port.

12. The system of Claim 1 wherein the switchable means for sharing a first set of common system resources includes:

one or more user input ports;

switch means for selectably connecting a respective user input signal from the user input port to either the first independent microcomputer system or to the second independent microcomputer system.

13. The system of Claim 12 wherein one of the user input port includes a keyboard port.

14. The system of Claim 12 wherein one of the user input port includes a mouse port.

15. The system of Claim 1 wherein the switchable means for sharing a first set of common system resources includes one or more serial communication ports.

16. The system of Claim 15 including:

a transceiver for receiving serial communication signals from either the first independent microcomputer system or from the second independent microcomputer system.

17. The system of Claim 15 wherein the one or more serial communication ports includes a modem port.

18. The system of Claim 15 wherein the one or more serial communication ports includes a printer port.

19. The system of Claim 1 wherein the switchable means for sharing a first set of common system resources includes a main memory port.

20. The system of Claim 1 wherein the means for connecting a second set of system resources to the first and the second independent microcomputer system includes one or more connector slots for connecting respective plug-in cards for the first and the second independent microcomputer systems.

21. The system of Claim 1 wherein the one or more connector slots for connecting respective plug-in cards for the first and the second independent microcomputer systems includes connector slots for a NUBUS bus system.

22. The system of Claim 1 wherein the one or more connector slots for connecting respective plug-in cards for the first and the second independent microcomputer systems includes connector slots for a ISA bus system.

23. The system of Claim 1 wherein the means for connecting a second set of system resources to the first and the second independent microcomputer system includes terminals for one or more floppy disk drives compatible with the first and the second independent microcomputer systems.

24. A method for alternatively sharing common system resources with two independent microcomputer systems, comprising the steps of:

connecting a first microcomputer system to the common system resources using switchable connection means;

booting up the first microcomputer system with the common system resources being connected thereto;

removing the common system resources from the first microcomputer system;

maintaining the first microcomputer system operational with the common system resources being removed therefrom;

connecting a second microcomputer system to the common system resources using switchable connection means;;

booting up the second microcomputer system with the common system resources being connected thereto;

maintaining the second microcomputer system operational with the common system resources being removed therefrom;

activating the switchable connection means to selectably connect the common system resources to either the first microcomputer system or to the second microcomputer system.

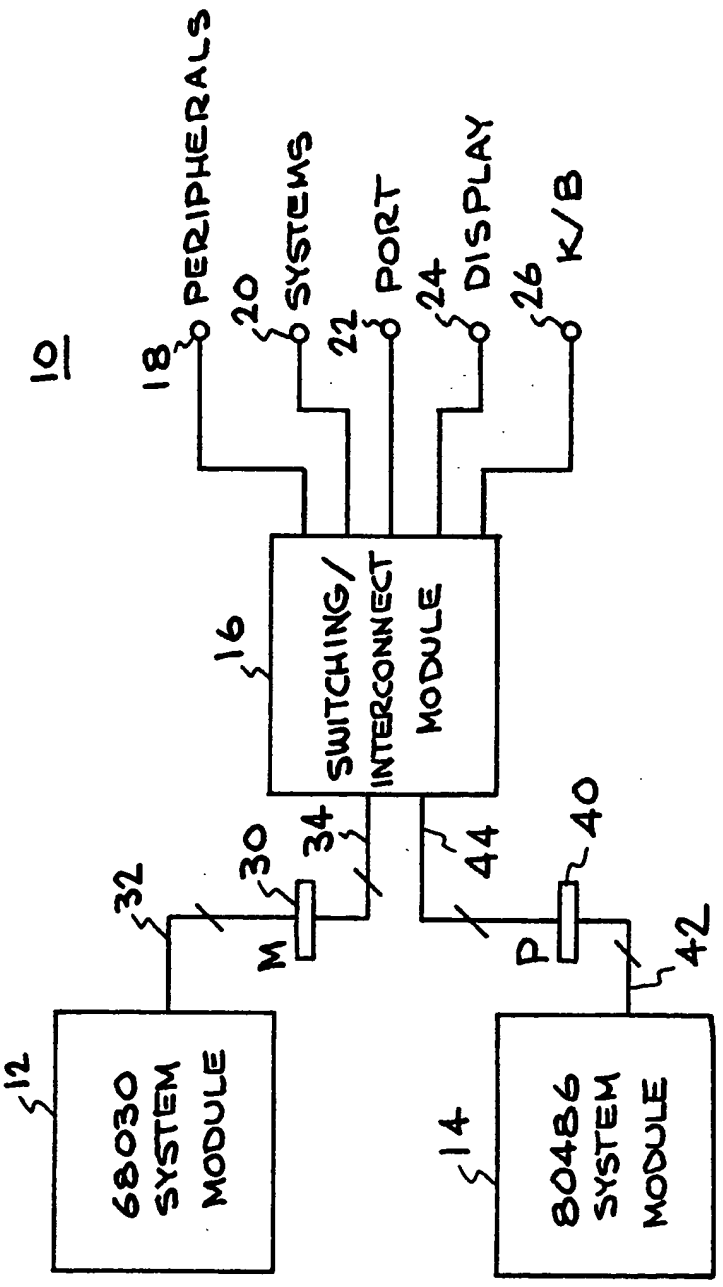

10
18
PERIPHERALS
20
SYSTEMS
22
PORT
24
DISPLAY
26
K/B
16
SWITCHING/
INTERCONNECT
MODULE
30
34
32
M
44
40
P
42
12
68030
SYSTEM
MODULE
14
80486
SYSTEM
MODULE

FIG. 1

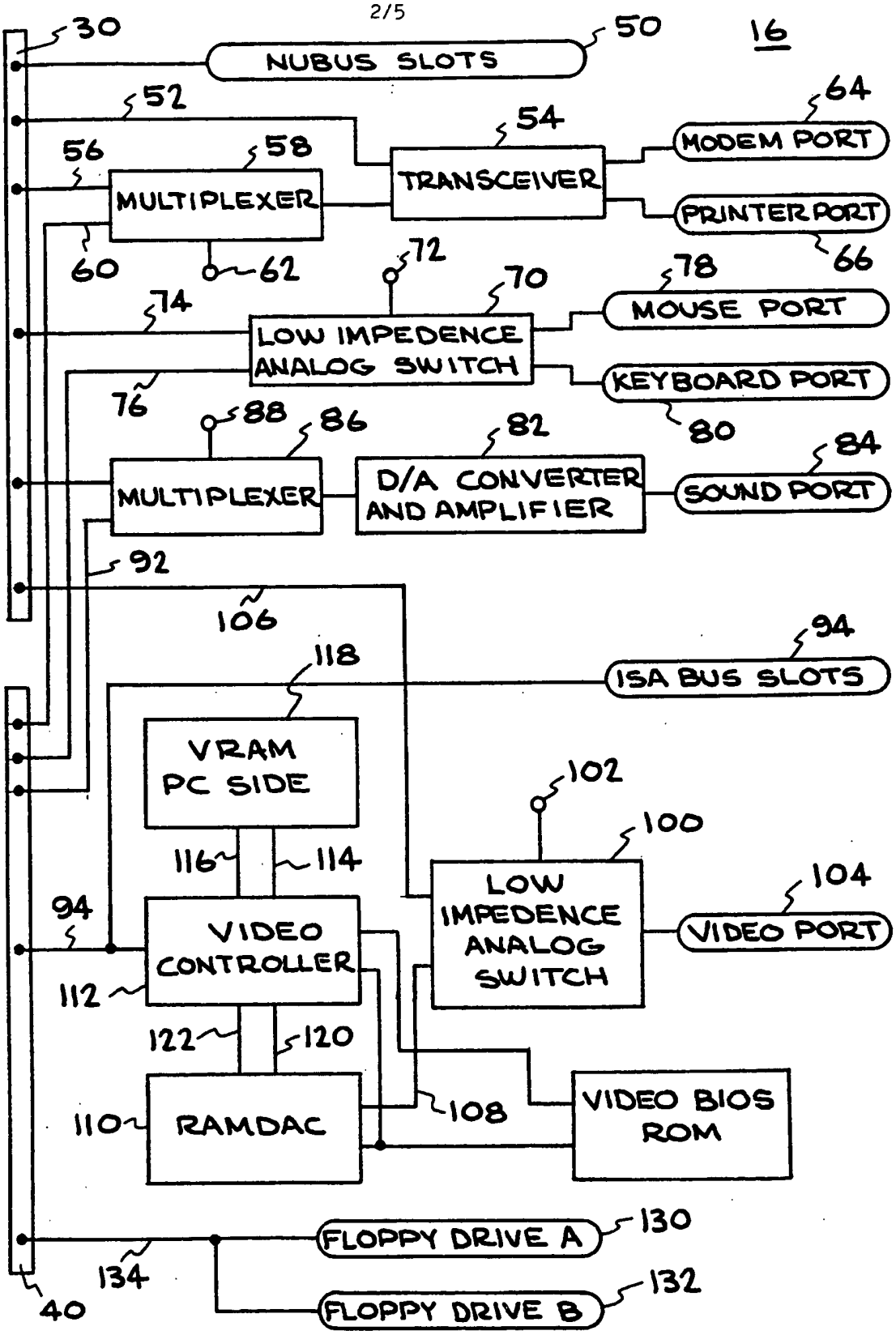

16
30
NUBUS SLOTS
50
52
54
64
MODEM PORT
56
58
TRANSCEIVER
MULTIPLEXER
PRINTER PORT
66
60
62
72
70
78
74
MOUSE PORT
LOW IMPEDENCE ANALOG SWITCH
KEYBOARD PORT
76
80
88
86
82
84
MULTIPLEXER
D/A CONVERTER AND AMPLIFIER
SOUND PORT
92
106
94
118
ISA BUS SLOTS
VRAM PC SIDE
102
100
116
114
LOW IMPEDENCE ANALOG SWITCH
104
94
VIDEO CONTROLLER
VIDEO PORT
112
122
120
110
RAMDAC
108
VIDEO BIOS ROM
130
FLOPPY DRIVE A
134
132
40
FLOPPY DRIVE B

FIG. 2

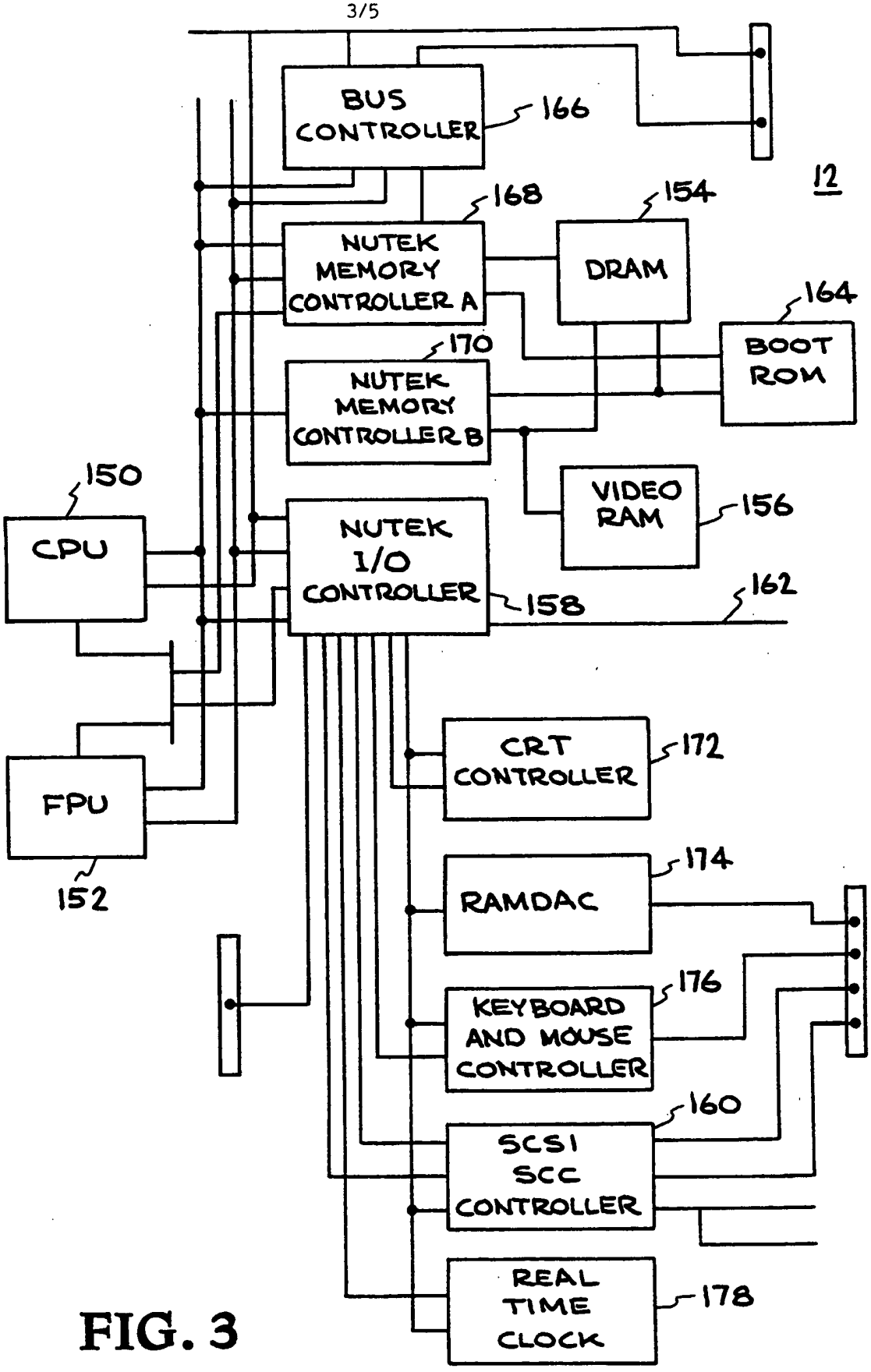

BUS CONTROLLER
166
12
168
154
NUTEK MEMORY CONTROLLER A
DRAM
164
BOOT ROM
170
NUTEK MEMORY CONTROLLER B
150
VIDEO RAM
156
CPU
NUTEK I/O CONTROLLER
158
162
CRT CONTROLLER
172
FPU
152
RAMDAC
174
176
KEYBOARD AND MOUSE CONTROLLER
160
SCSI SCC CONTROLLER
REAL TIME CLOCK
178

FIG. 3

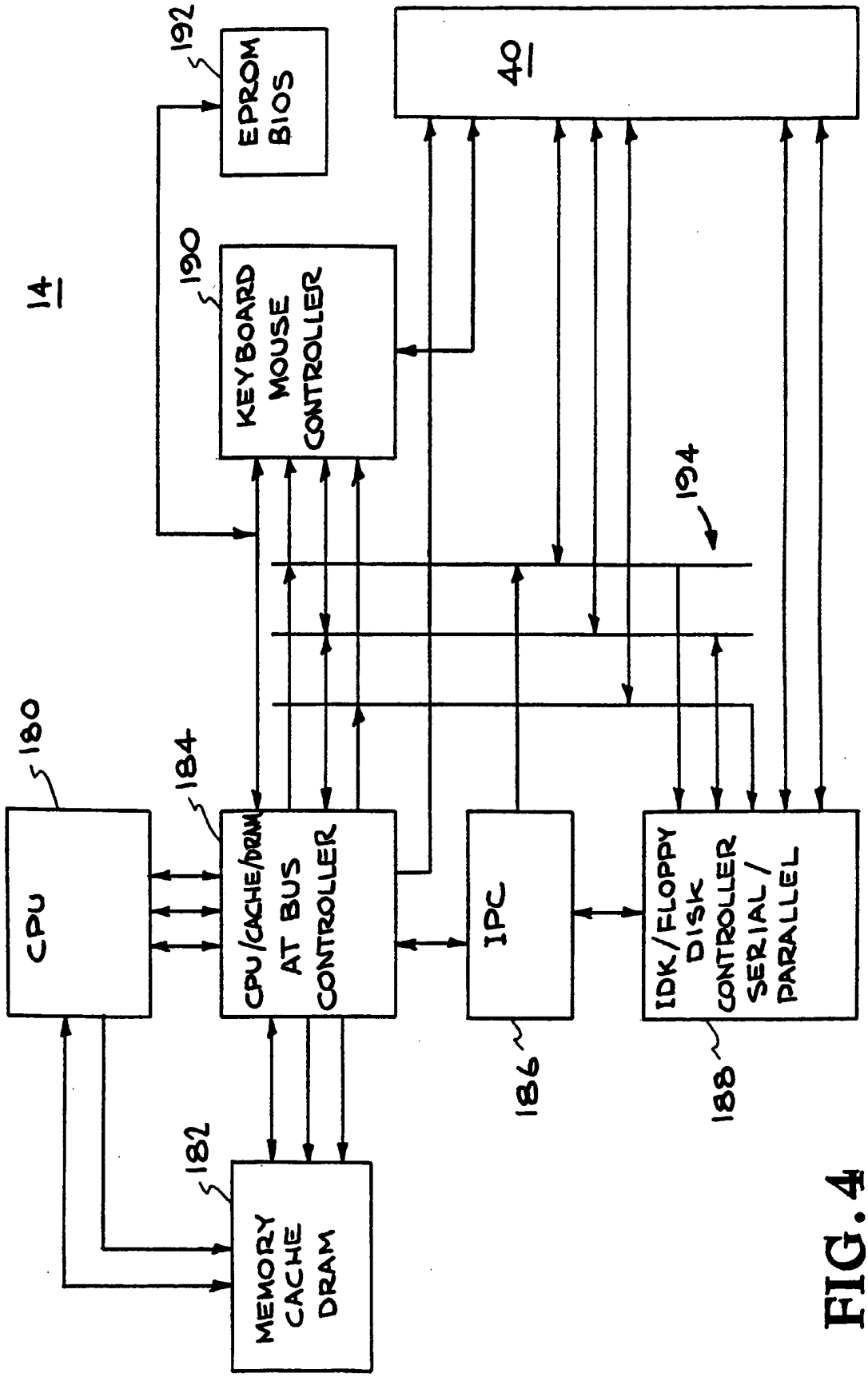

14
40
192
EPROM BIOS
190
KEYBOARD MOUSE CONTROLLER
194
180
CPU
184
CPU/CACHE/DRAM AT BUS CONTROLLER
IPC
IDK/FLOPPY DISK CONTROLLER SERIAL/ PARALLEL
182
MEMORY CACHE DRAM
186
188

FIG. 4

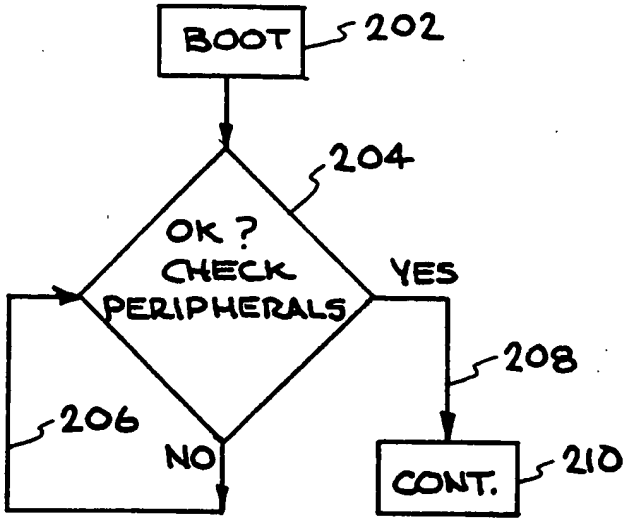

BOOT
202
204
OK ?
CHECK
PERIPHERALS
YES
208
206
NO
CONT.
210

FIG. 5

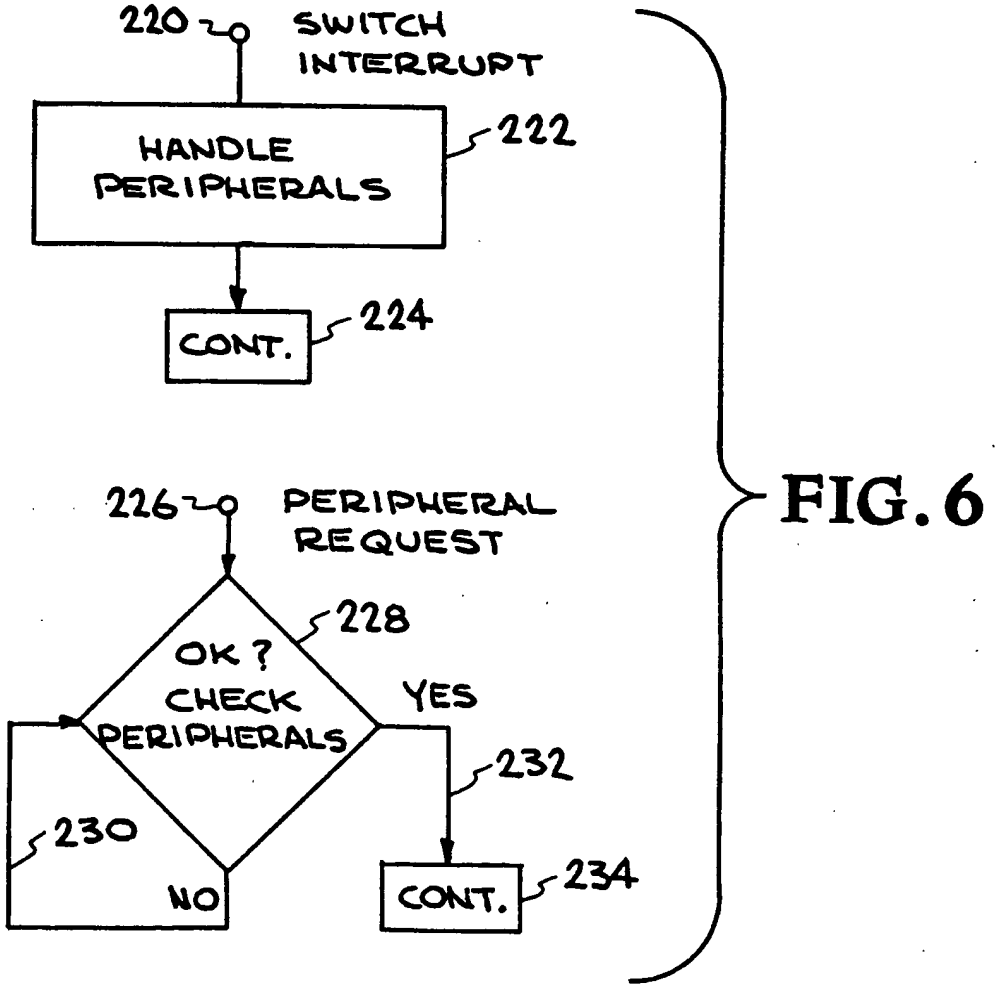

220
SWITCH
INTERRUPT
HANDLE
PERIPHERALS
222
CONT.
224
226
PERIPHERAL
REQUEST
228
OK ?
CHECK
PERIPHERALS
YES
232
230
NO
CONT.
234

FIG. 6

INTERNATIONAL SEARCH REPORT

Int onal Application No
PCT/US 93/10351

A. CLASSIFICATION OF SUBJECT MATTER
IPC 5 G06F13/40

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 5 G06F

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	COMPUTER STANDARDS AND INTERFACES, vol.5, no.1, 1986, AMSTERDAM NL pages 47 - 53 HALDAR ET AL. 'A circuit for sharing peripherals and instruments with the IEEE-488 interface between two or more microcomputers' see abstract; figure 1 ---	1-4,6-23
Y	EP,A,0 130 733 (FUJITSU LTD.) 9 January 1985 see page 1, line 19 - page 4, line 6; figure 1 see page 9, line 11 - page 10, line 15; figure 3 --- -/--	1-4,6-23

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
28 February 1994	09.06.94
Name and mailing address of the ISA European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax (+31-70) 340-3016	Authorized officer JONES H.D.

Form PCT/ISA/210 (second sheet) (July 1992)

INTERNATIONAL SEARCH REPORT

Int. ional Application No
PCT/US 93/10351

C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	US,A,4 608 663 (GORDON) 26 August 1986 see column 3, line 13 - column 4, line 16; figures 1,2	1-3,7, 10-12
A	EP,A,0 359 064 (HEWLETT-PACKARD COMPANY) 21 March 1990 see page 2, column 2, line 22 - page 3, column 3, line 29; figures 1,2A,2B	1-4, 13-20
A	EP,A,0 483 865 (KABUSHIKI KAISHA TOSHIBA) 6 May 1992 see page 2, column 2, line 50 - page 3, column 4, line 22; figure 1	8,13-23

2

INTERNATIONAL SEARCH REPORT

...ernational application No.
PCT/US93/10351

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see annexed sheet

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searches without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☒ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

1-23

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☐ No protest accompanied the payment of additional search fees.

INVITATION TO PAY ADDITIONAL FEES

International application No.
PCT/US93/10351

1. Claims 1-23 : Switchable multi-microcomputers with shared resources.

2. Claim 24 : Booting procedure.

The special technical feature of the first invention is:

switchabel multi-microcomputers with shared resources.

According to rule 13 PCT non.unity a priori is detected for invention 2 which mainly deals with a booting procedure. As a result, there is no technical link between the 2 inventions.

INTERNATIONAL SEARCH REPORT

information on patent family members

Int. ional Application No
PCT/US 93/10351

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
EP-A-0130733	09-01-85	JP-B-	1008387	14-02-89
		JP-C-	1526387	30-10-89
		JP-A-	60008972	17-01-85
		US-A-	4716526	29-12-87
US-A-4608663	26-08-86	NONE		
EP-A-0359064	21-03-90	JP-A-	2114311	26-04-90
EP-A-0483865	06-05-92	JP-A-	4169929	17-06-92
		JP-A-	4205627	27-07-92
		US-A-	5274816	28-12-93